APPLICATION NOTE

Programmable Handheld Calculator Computes Digital-to-Analog Converter Errors

With input data provided from a simple test setup, a convenient program has been coded for the SR-52 handheld calculator, with or without a PC-100A printer, to quickly and easily compute and record offset, gain, and linearity errors of a binary-coded D-A converter that has a resolution of 12 bits or less

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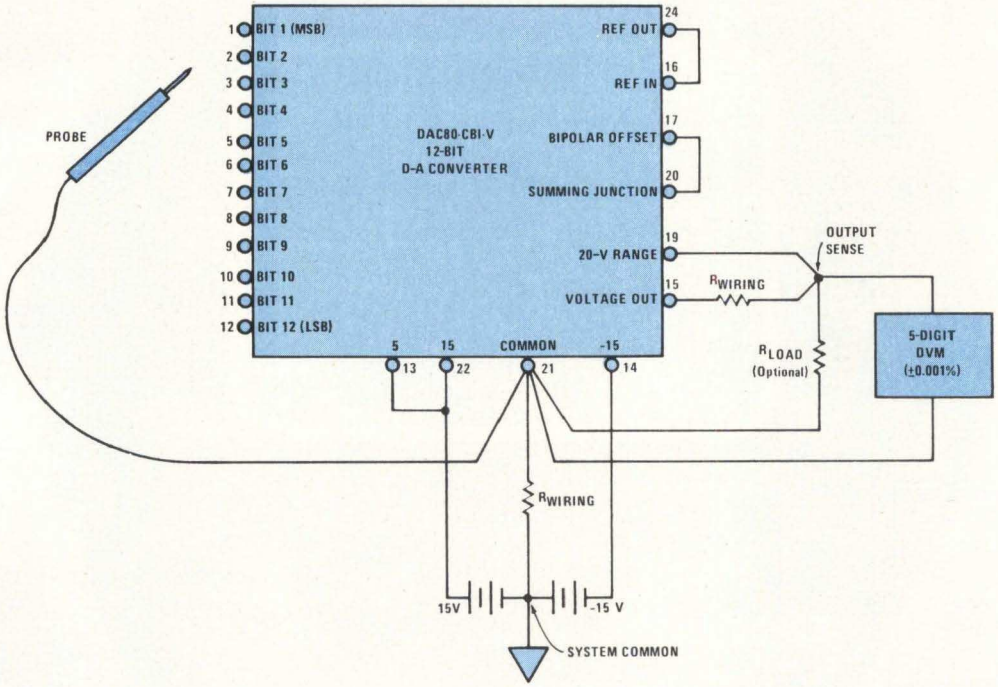
The total error of a digital-to-analog converter is most meaningfully expressed as the sum of three error components: offset or minus full scale error, gain error, and linearity error. Offset error is the deviation of the actual converter's all bits off output value (V_{-FS}) from the all bits off output value of an ideal converter. Gain error is the difference between the actual output span [all bits on output value (V_{FS}) minus the all bits off output value] and the ideal output span; initial gain and offset errors can easily be eliminated in many applications with external potentiometers. Linearity error is the deviation of the analog output value relative to the straight line drawn between the all bits off and the all bits on output values. Sometimes called relative accuracy, linearity error is the true measure of digital-to-analog converter performance because it cannot be adjusted externally; this error is usually specified in terms of least significant bits (LSBs), where one LSB is equal to $(V_{FS} - V_{-FS})/(2^n - 1)$, and n equals the number of digital input lines or bits. Most digital-to-analog converter applications require a linearity error of less than $\pm\frac{1}{2}$ LSB for any digital input code to ensure that the output will be monotonic (ie, the analog output will increase or remain the same for an increasing digital input code).

A program has been developed for an SR-52* programmable calculator and PC-100A printer to allow a designer to rapidly evaluate and record the error performance of a binary-coded digital-to-analog converter (DAC) with a minimum amount of input data. The user enters into the calculator the output voltage or current value obtained by turning each bit on by itself, beginning with the most significant bit (MSB). The SR-52 automatically calculates and prints the offset error [% of full scale range (FSR)], gain error (%), and linearity error (in both LSBs and volts), as well as the worst-case linearity error (in LSBs) and associated digital input code. It requires less than one minute to execute the calculator program for a 12-bit DAC. The program can be modified easily for use without the printer.



DAC test setup. Each bit line is connected to ground one at a time beginning with MSB. Output voltage noted on voltmeter is entered into SR-52 calculator to provide complete dc error analysis of 12-bit DAC in less than 1 min. Only minimum input data are needed; results are given in units common to most major converter types

Test Setup

The test setup in the Figure is applied to the DAC80-CB1-V 12-bit DAC; however, the program will operate for any binary-coded DAC with a resolution of 12 bits or less. Necessary test equipment includes a regulated (±0.1%) power supply of ±15 V (other DACs may require different voltages), and a digital voltmeter (DVM) whose accuracy is at least 10 times better than the linearity of the converter being tested; ½ LSB is about 0.012% of the FSR for a 12-bit DAC. Therefore, a 5-digit DVM (accuracy = ±0.001%) is required.

Since the digital input code of the DAC80 is complementary binary (a 0 on a digital input line turns that bit on), all that is necessary is to simply connect each bit to ground one at a time beginning with the MSB; the voltmeter reading is noted, and the output voltage is entered into the calculator. The only other information required is the FSR

TABLE 1

SR-52 User Instructions for 12-Bit DAC Error Analysis Program

Step	Procedure	Enter	Press	Display
1.0	Load program card (sides A and B)			
2.0	Initialize		E	1.0000
3.0	Input data			
3.1	Enter full scale range	V_{FSR}	B	V_{FSR}
3.2	Enter minus full scale (ideal)	$V_{-FS\ ideal}$	C	$V_{-FS\ ideal}$
3.3	Enter minus full scale (actual)	$V_{-FS\ actual}$	D	$V_{-FS\ actual}$
3.4	Enter output value obtained with each bit turned on by itself (begin with MSB)	Vob_i	A	1.0000
3.5	Repeat 3.4 for each bit (12 bits max)			
4.0	Calculate D-A errors		Run	Worst-case binary code

Error Analysis Printout for 12-Bit DAC

INPUT	FULL SCALE RANGE	20.0000
	IDEAL (ALL BITS OFF)	10.0000
	ACTUAL (ALL BITS OFF)	-9.9973
	BIT 1 VOLTAGE (MSB)	0.0004
	BIT 2	-4.9985
	BIT 3	-7.4980
	BIT 4	-8.7478
	BIT 5	-9.3718
	BIT 6	-9.6848
	BIT 7	-9.8410
	BIT 8	-9.9193
	BIT 9	-9.9585
	BIT 10	-9.9780
	BIT 11	-9.9878
	BIT 12 (LSB)	-9.9926
OUTPUT	OFFSET ERROR (% OF FSR)	0.0135
	GAIN ERROR (%)	-0.0261
	LINEARITY ERROR (GAIN AND OFFSET ERROR ELIMINATED)	
	BIT 1 (VOLTS)	0.0003
	(LSB S)	0.0633
	BIT 2 (VOLTS)	0.0001
	(LSB S)	0.0214
	BIT 3 (VOLTS)	0.0000
	(LSB S)	-0.0098
	BIT 4 (VOLTS)	-0.0002
	(LSB S)	-0.0356
	BIT 5 (VOLTS)	0.0007
	(LSB S)	0.1358
	BIT 6 (VOLTS)	0.0001
	(LSB S)	0.0167
	BIT 7 (VOLTS)	0.0001
	(LSB S)	0.0186
	BIT 8 (VOLTS)	-0.0001
	(LSB S)	-0.0214
	BIT 9 (VOLTS)	-0.0003
	(LSB S)	-0.0517
	BIT 10 (VOLTS)	-0.0002
	(LSB S)	-0.0463
	BIT 11 (VOLTS)	-0.0003
	(LSB S)	-0.0539
	BIT 12 (VOLTS)	-0.0002
	(LSB S)	-0.0372
	W.C. LINEARITY ER. (LSB)	0.2559
	WORST CASE CODE	3296.0000

TABLE 2

SR-52 Coding Form for 12-Bit DAC Error Analysis Program

Loc	Code	Key	Loc	Code	Key	Loc	Code	Key
000	43	RCL		65	X		98	prt
	01	1		43	RCL	075	99	pap
	06	6		01	1		99	pap
	75	−	040	06	6		43	RCL
	43	RCL		94	+/−		01	1
005	01	1		85	+		07	7
	05	5		43	RCL	080	85	+
	95	=		01	1		01	1
	42	STO	045	07	7		95	=
	01	1		75	−		20	1/x
010	08	8		43	RCL		65	X
	55	÷		01	1	085	53	C
	43	RCL		04	4		36	IND
	01	1	050	85	+		43	RCL
	04	4		43	RCL		06	6
015	65	X		01	1		09	9
	01	1		04	4	090	75	−
	00	0		55	÷		43	RCL
	00	0	055	02	2		01	1
	95	=		45	Y^x		06	6
020	99	pap		43	RCL		54	)
	98	prt		09	9	095	95	=
	43	RCL		08	8		75	−
	09	9	060	95	=		43	RCL
	09	9		55	÷		01	1
025	75	−		43	RCL		04	4
	01	1		01	1	100	55	÷
	42	STO		04	4		02	2
	06	6	065	95	=		45	Y^x
	09	9		42	STO		43	RCL
030	95	=		01	1		06	6
	42	STO		07	7	105	09	9
	09	9		65	X		95	=
	08	8	070	01	1		98	prt
	42	STO		00	0		65	X
035	00	0		00	0		02	2
	00	0		95	=	110	45	Y^x

(10 V for a 0- to 10-V output or 20 V for a ±10-V output, for example), the ideal minus full scale or all bits off voltage (0 V for a 0- to 10-V output or −10 V for a ±10-V output, for instance), and the actual all bits off value. No adjustments of gain or offset errors are required for computing linearity error since the calculator automatically computes a "best-fit" straight line between the all bits on and all bits off output values of the DAC. Actual input and output data obtained with this test method and the printer are shown in the Error Analysis Printout for 12-Bit DAC.

Error Analysis Program Equations

$$\text{Offset Voltage } (V_{OS}) = V_{-FS\ actual} - V_{-FS\ ideal}$$

$$\text{Offset Error (\% of FSR)} = \frac{V_{OS}}{V_{FSR\ ideal}} \times 100$$

$$\text{Gain Error} = \Delta K = \frac{V_{FSR\ actual} - V_{FSR\ ideal}}{V_{FSR\ ideal}}$$

$$= \frac{\left[\sum_{i=1}^{n} Vob_i - nV_{-FS\ actual}\right] - \left[V_{FSR\ ideal} - \frac{V_{FSR\ ideal}}{2^n}\right]}{V_{FSR\ ideal}}$$

where: V_{FSR} = full scale range

n = number of bits

Loc	Code	Key	Loc	Code	Key	Loc	Code	Key
	43	RCL		06	6	177	01	1
112	09	9		09	9		06	6
	08	8		58	dsz		98	prt
	55	÷	147	00	0		99	pap
	43	RCL		07	7		81	HLT
	01	1		07	7	182	46	LBL
117	04	4		99	pap		11	A
	95	=		43	RCL		98	prt
	98	prt	152	01	1		36	IND
	99	pap		03	3		42	STO
	22	INV		98	prt	187	09	9
122	80	if pos		43	RCL		09	9
	01	1		01	1		44	SUM
	04	4	157	09	9		01	1
	02	2		98	prt		07	7
	44	SUM		81	HLT	192	01	1
127	01	1		46	LBL		44	SUM
	03	3		12	B		09	9
	02	2	162	42	STO		09	9
	45	Y^x		01	1		81	HLT
	53	(		04	4	197	86	rset
132	43	RCL		98	prt		46	LBL
	00	0		81	HLT		15	E
	00	0	167	46	LBL		25	CLR
	75	−		13	C		47	CMS
	01	1		42	STO	202	57	fix
137	54	)		01	1		04	4
	95	=		05	5		01	1
	44	SUM	172	98	prt		42	STO
	01	1		81	HLT		09	9
	09	9		46	LBL	207	09	9
142	01	1		14	D		81	HLT
	44	SUM		42	STO			

Labels: A = bit values, B = FSR, C = −FS ideal, D = −FS actual, E = initialize

Registers: 00 = bit counter, 01 = bit 1 value, 02 = bit 2 value, 03 = bit 3 value, 04 = bit 4 value, 05 = bit 5 value, 06 = bit 6 value, 07 = bit 7 value, 08 = bit 8 value, 09 = bit 9 value, 10 = bit 10 value, 11 = bit 11 value, 12 = bit 12 value, 13 = worst-case linearity error, 14 = FSR, 15 = −FS ideal, 16 = −FS actual, 17 = gain error, 18 = V_{os}, 19 = worst-case code, 69 = counter, 98 = n (# of bits), 99 = counter

Vob_i = individual bit output voltage or current

Gain error (%) = $\Delta K \times 100$

Bit error (volts) = $E_i = \frac{1}{1 + \Delta K}(Vob_i - V_{-FS\ actual}) - \frac{V_{FSR\ ideal}}{2^i}$

Bit error (LSB) = $\epsilon_i = \frac{E_i \times 2^n}{V_{FSR\ ideal}}$

Total linearity error (LSB) = $\sum_{i=1}^{n} \epsilon_i, (\epsilon_i > 0)$

Worst-case code (decimal) = $\sum_{i=1}^{n} 2^i, (\epsilon_i > 0)$

User Instructions

Concise user instructions[1] for the programmable calculator are listed in Table 1; the SR-52 coding form for the DAC error analysis program is shown in Table 2. The computations performed by the program are listed under the Error Analysis Program Equations.

An implicit assumption in the calculation of total linearity error and worst-case code is that the individual bit errors are not interdependent; that is, the contribution to the output value of each individual bit should not change when the other bits are turned on or off.[2] If the contribution to the output value of each bit is dependent upon whether the other bits are turned on or off, the converter is said to exhibit superposition error. Almost all DACs exhibit a slight superposition error due to thermal gradients or critical currents sharing a common ground path; but as long as it is less than 1/10 LSB, it can be neglected. This error is almost always negligible for well-designed discrete, hybrid, or monolithic DACs that have a resolution of 12 bits or less.

The PC-100A printer provides a convenient hard copy of all input and output data. To use the program without the printer, replace the print statements (prt) at calculator memory locations 021, 074, 107, 119, and 154 with halt statements (HLT). The results will be displayed in the same order as shown in the Error Analysis Printout. Simply press run after recording each result.

This program can check the accuracy of DACs used in automatic or manual test equipment, process control, or data processing to determine quickly whether calibration is required. Another application is to check DACs on an incoming inspection basis to ensure that critical parameters are being met.

References

1. "SR-52 Owner's Manual," Texas Instruments, Inc, Dallas, Texas, 1975
2. T. Cate, "Tom Cate of Burr-Brown speaks out on D/A converter specs," *EDN*, June 1, 1971, pp 34-40

*Interested readers may obtain a copy of Mr Prazak's program for the TI-59 calculator by requesting it in writing from the Editor, *Computer Design* magazine.