TI 59-58 hardware annotations

Introduction

This is the annotation file that accompanies the TI59/58 hardware diagrams available on my web-site http://xgistor.ath.cx

This information is based upon material written in Dutch by M.B. van der Mark in 1982. This material was made as a school project at the time. I have never met Mr. van der Mark but I suspect that I am following his wishes if I preserve his legacy for future generations, by making it available on the world wide web. His thesis did not contain any legal or other restrictions for me not doing so.

Initially I will not translate all the material he has provided in this thesis, just the bare bones of the TI59 operation and a description of the signals, timings and some other internals, revamped by color full and comprehensible diagrams and what ever I can phantom myself but what was not directly obvious from the source material.

However, my rule of thumb for now is that I will write only about things I understand, this because some of the original information was put down in a somewhat ambiguous fashion with some loose ends that I cannot resolve at this moment. M.B. van der Mark occasionally referred back to previously written material that I have no access to right now.

The annotation and the diagrams for the PC100 printer will be available (soon) in a separate set of files.

Anybody who is willing and able to provide additional material is invited to provide me with such and I will further process all material and make revisions on this information, to be put in the public domain as soon as reasonably possible.

Eventually I would also like to enhance this material with stuff about the “**HIR-commands**” and things like “**Fast-mode**” and “**Hex-programming**”. If you have any of this please let me know.

My ultimate goal would be to gather and concentrate enough information to enable a group of people to write a comprehensive emulator for the TI59/58. This would preserve this beautiful vintage calculator -in a virtual manner- for our offspring in the eons ahead.

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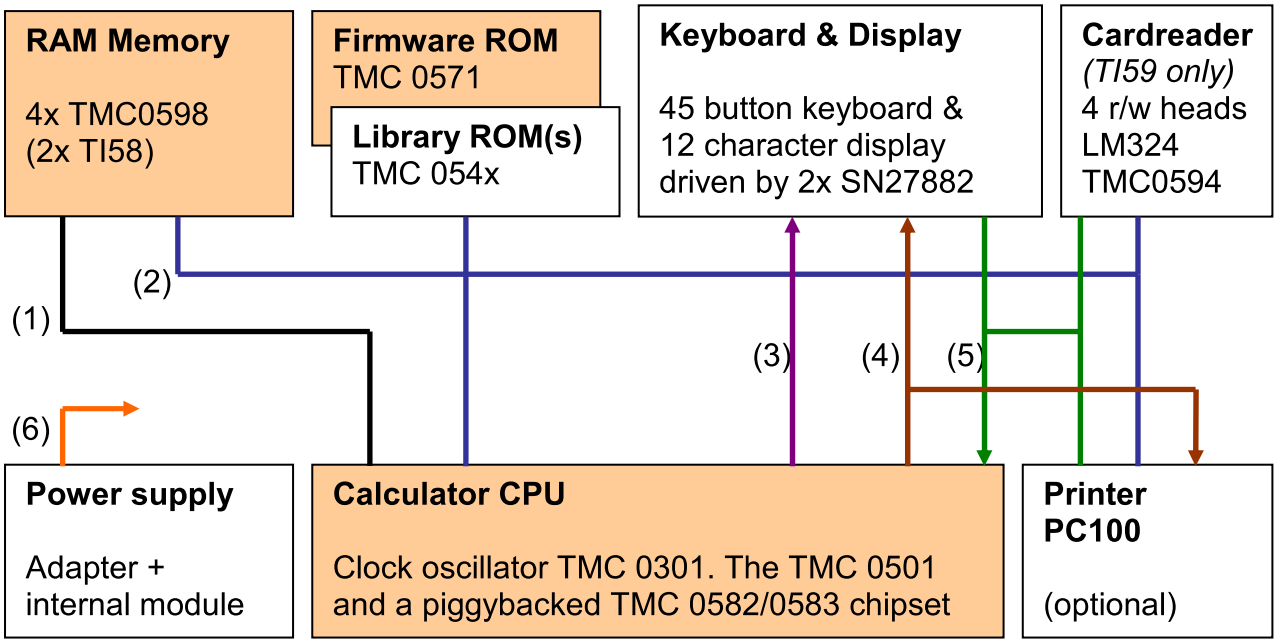
TI59/58 Block Diagram



Busses:

1. **I/O-1,I/O-2,I/O-4,I/O-8** ➔ **4 bits Databus (Tristate)**
2. **IDLE, φ1 & φ2, EXT, IRG** ➔ **Sync, Timing&Control and serial data&instruction bus**
3. **SA … SG + DPT** ➔ **S-BUS segment lines**
4. **D0 … D15, *(L0 ..L12)*** ➔ **D-BUS scanning lines *(L= digit driver lines)* (output)**
5. **KN … KT** ➔ **K-BUS scanning return lines (input)**
6. **Vss, -Vbat, Vdd, Vgg** ➔ **Power supply lines 0V, -3,7V, -10V, -15,7V resp.**

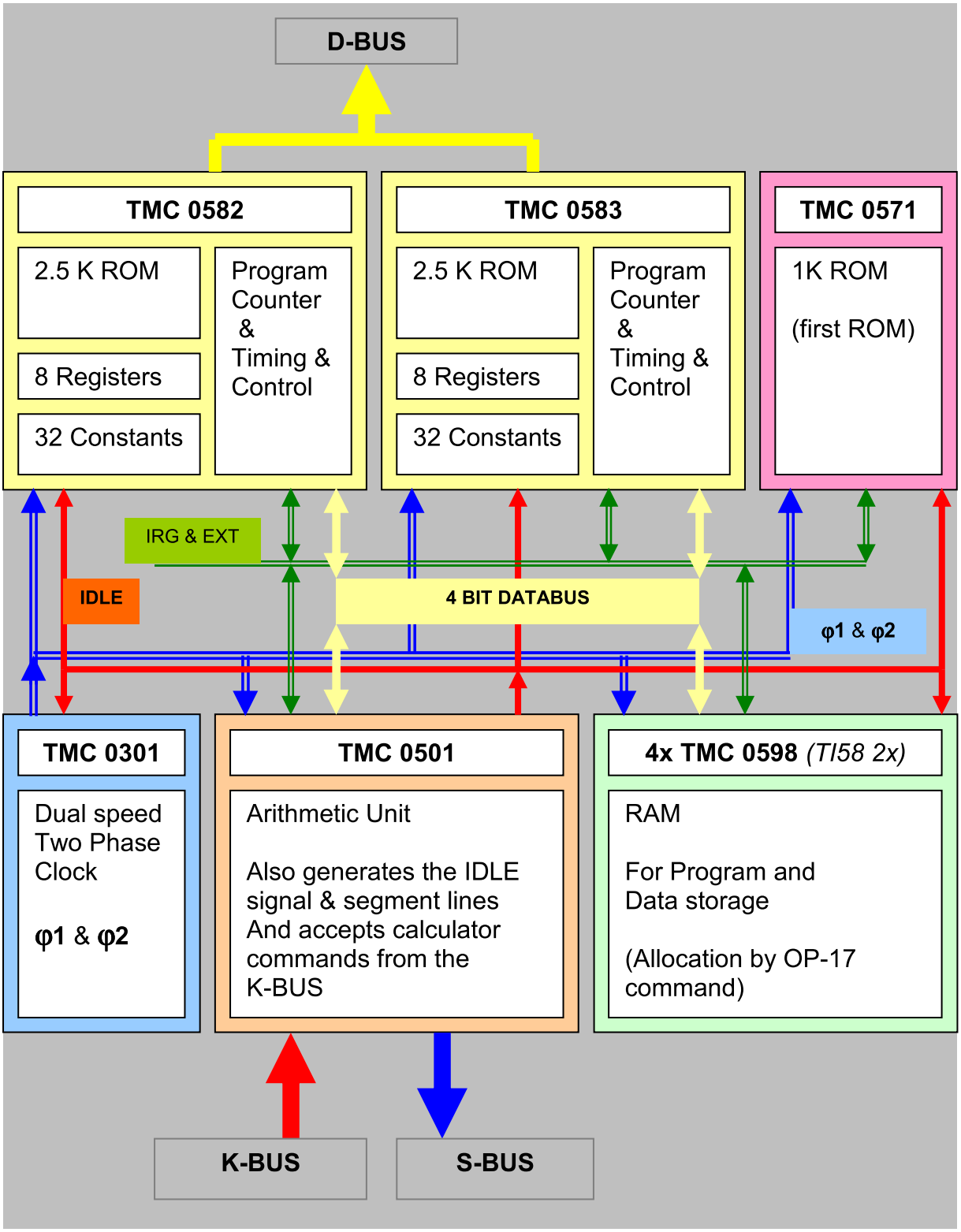
(input/output designation with respect to the CPU)

I suspect that all the TMC-chips are PMOS-technology, this based on the fact that they all require special extra negative power supply with respect to the main battery power. There is a thick-film power module in the calculator that provides for these extra voltages.

> **Warning! Since this power module does not contain any kind of voltage regulation I strongly advise you not operate the calculator without the battery package. The output of this power module may run out of control and may generate voltages that the PMOS-chips may not survive! In effect the batteries themselves act like a voltage regulator. (This is a feature of many calculators from the PMOS era, so be warned!)**

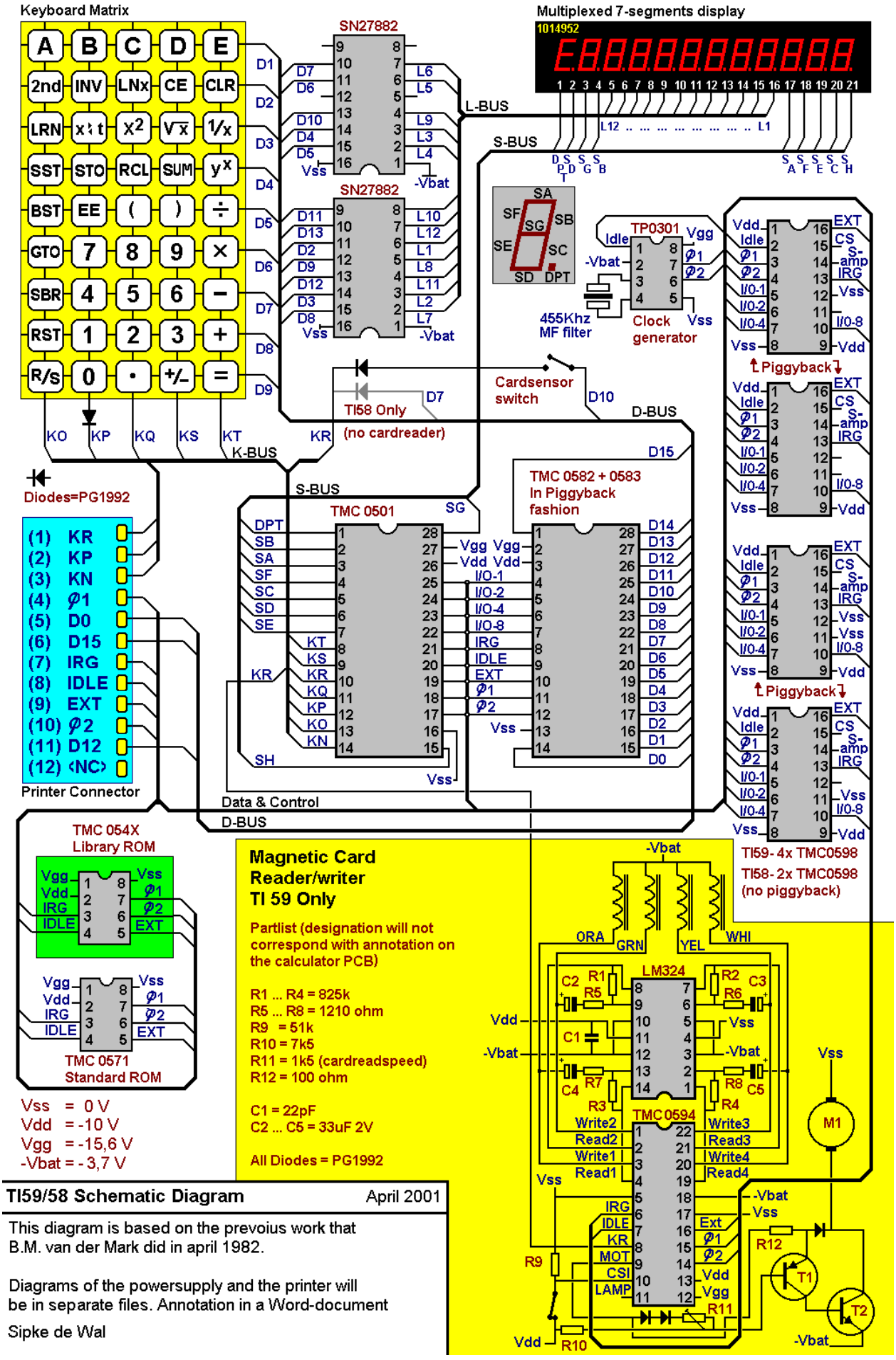
Before we'll cover the block diagram we'll need to know more about the role of the individual chips that form the processing core of the calculator. In the above diagram shown as the shaded parts. The rest of the machine can be regarded as peripheral devices with respect to the CPU-core. To understand it's operation we need to examine what functions are actually implemented in the core and how they are interwoven by the various types of signals.

CPU Corechips



Based on the above diagram we may conclude there are two sets of signal-busses in the TI59.

- The Data&Control-bus that glue the chipset together and additionally interfaces with the library-ROM, the Card Reader and the Printer. Most of the “internal” data and instructions are transmitted serially only the numerical data and the user-programming code are exchanged between the CPU and the RAM-chips by means of a 4-BIT unidirectional data bus.
- The D-, S-, K-Scanning busses interface with the keyboard and the LED-Display. By way of exception one of the K-lines (KR) is used as a BUSY line that is utilized by the Card Reader and the Printer to indicate their busy-state to the CPU.



TI59/58 Schematic Diagram April 2001

This diagram is based on the prevoius work that B.M. van der Mark did in april 1982.

Diagrams of the powersupply and the printer will be in separate files. Annotation in a Word-document

Sipke de Wal

The previous page shows a small version of the TI59/58 diagram (A larger version is available at my web-site)

Busses:

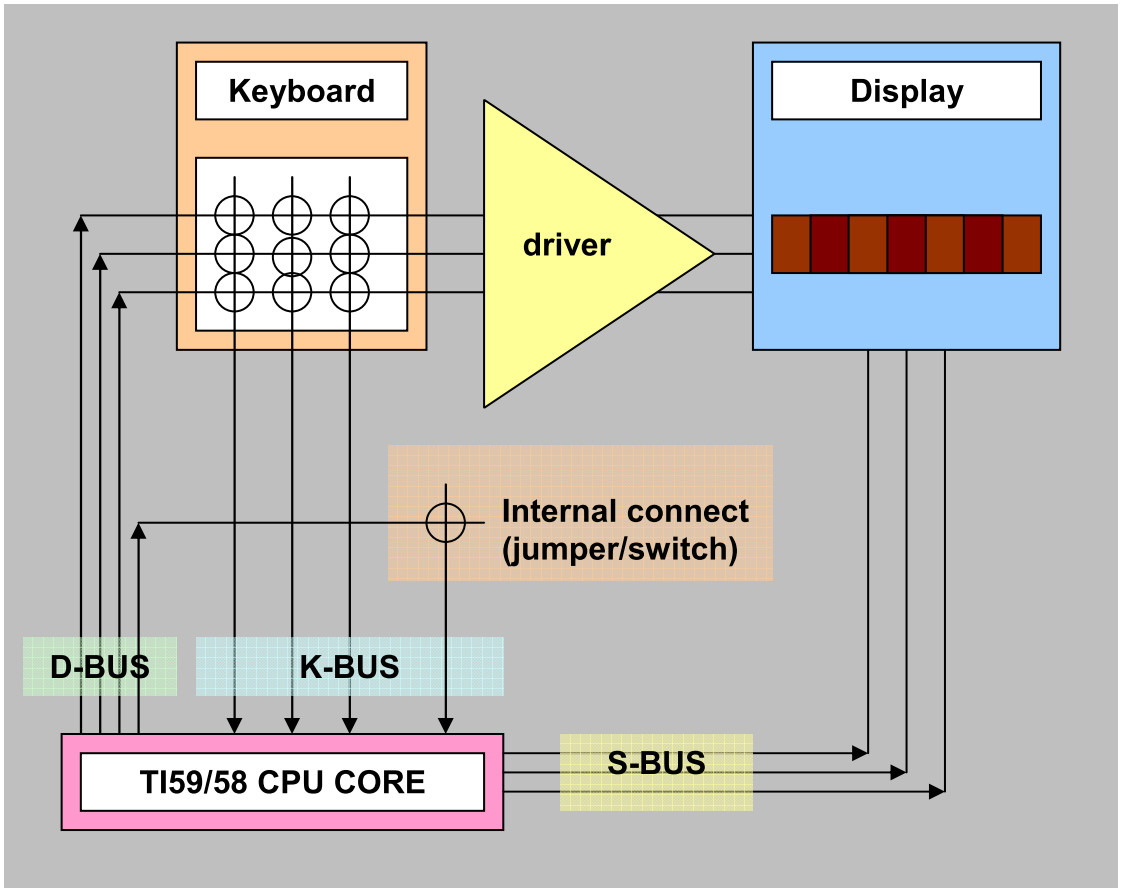
Data & Control	φ1 & φ2 Clock signals	This is a 2-phase (non-overlapping) clock that switches between Vss and Vgg. It is derived from a 455 KHZ MF filter through the TMC0301-chip but some models of the TI59 have deviating ratings like 462 KHZ. The Clock operates in two modes. • Calculating (full speed) • Display or IDLE-mode (low speed) A Clock pulse is active at the negative Vgg level and each pulse takes 1.1 μSec. Then in IDLE-mode there is a pause of 3 cycles of the clock (See timing diagram) The period between two succeeding leading edges of φ1 are defined as a "State Time". 16 State-times make up and instruction-cycle. The first State-time of such a cycle is designated S0. Then S1, S2, S3 …..	Vss-Vgg (out)
	IDLE	IDLE indicates when the Arithmetic CHIP is finished with operations and a result is displayed. IDLE switches between Vss and Vdd. IDLE will always assert negative at the start S0. If trailing edge of IDLE goes up during S1 then the calculator is in Calculating mode and works at full speed. If the trailing edge of IDLE goes up at S15 this will then indicate that the Calculator is in Display or IDLE-mode This alteration of speeds facilitates longer pulses on the D-Scanning lines at display-time in order to make results more visible and also minimizes the power use of the CPU while the LEDs draw the most of the current. This evening out power use at all modes of operations.	Vss-Vdd (out)
	IRG	This is the serial instruction line. Although there are 16 bits transferred during S0 – S15 only the bits during S3-S15 are valid (S3=LSB). The first 2-bits are "DONT-CARE" The definitions of the instruction codes are described later on, in a couple of tables. IRG is a unidirectional (tri-state) line that switches between Vss and Vdd	Vss-Vdd (3ST)

	EXT	This is the serial data line. It functions similar to the IRG-line but valid bits are only transferred during S3 – S9 (S3=LSB) It also is unidirectional and also switches between Vss and Vdd. The EXT-line will transfer several types of data between the chips and character data to the Printer.	Vss-Vdd (3ST)
	I/O-1, I/O-2, I/O-4, I/O-8 Databus	These lines transfer BCD-digit data between the CPU and the RAM-chips. It could in principal transfer a few HEX-codes as well but there is not a lot of documentation on this. During the S0-S15 state-times (1 instruction cycle) a full 16-digit value can be transferred. Likewise 8 2-Digit user-programs steps can be transferred (See Value-representation Diagram) These lines switch between Vss and Vdd and are tri-state	Vss-Vdd (3ST)
Scanning busses	D0-D15	The are the Scan-send-lines. During subsequent instruction cycles each of the D-lines will go high (Vss) and stay high during that instruction cycle until S14. However, the leading edge of the D-signal will start during S15 in the previous instruction cycle The D-Lines scan the keyboard and some will be buffered to drive the Display LED-digits. (L-Bus). The D-lines will switch between Vss and Vdd, they are output only.	Vss-Vdd (out)
	L1 - L12	Derived from D2 –D13 these lines are buffered by 2 SN27882-chips to enhance the power output of the scan lines in order to drive the Display LED-digits. They switch between Vss and –Vbat	Vss--Vbat (out)
	KN – KT	These are the Scanning-return-lines with the exception of KR. They will connect to a D-line when a key is pressed on the keyboard and some extra K-lines are user as jumper or switch lines for special functions like the card reader enable and position switch and one to distinguish between a TI59 and a TI58 (Card Reader present or not) On some models a 1200 ohm resistor is placed in series with these lines. Some connections between D & K lines may lead to undocumented TI59/58 features like: KQ-D15=Master Reset KN-D5 … D11= Fast Mode/Firmware	(IN)

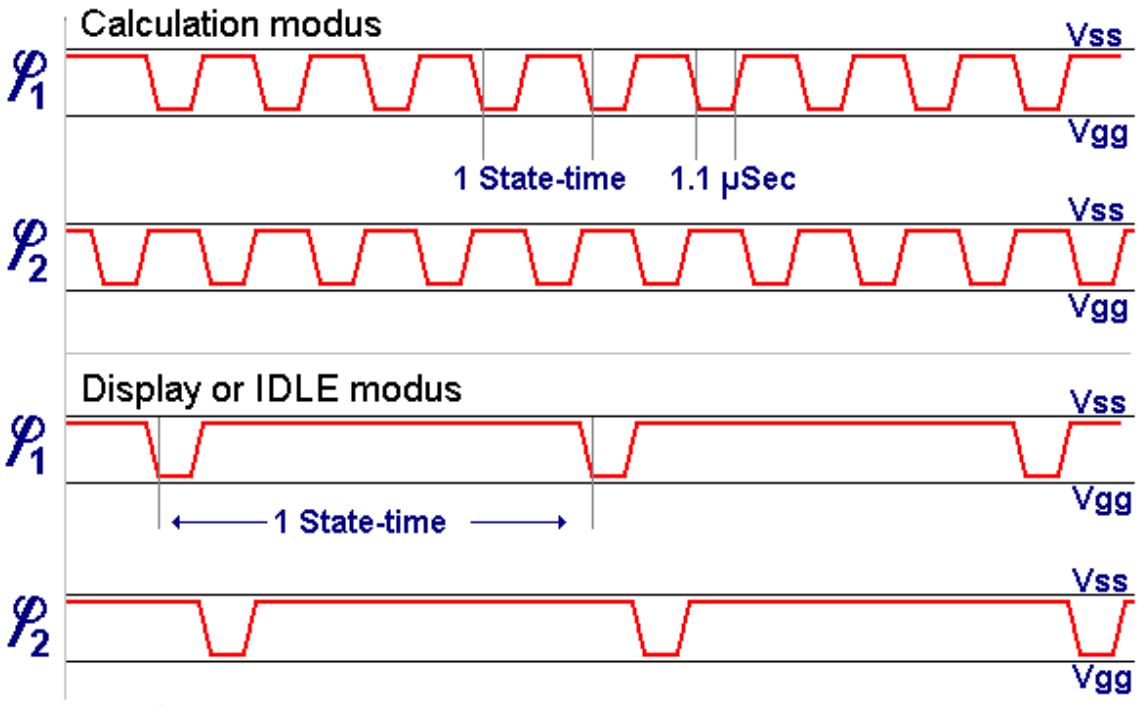
	BUSY (KR)	This Scan-return line is in effect a BUSY line for the Printer and the Card reader. The rest of the machine will wait as long as this line is held at Vss by a peripheral device		(IN)
	SA – SH & DPT	Segment-lines will drive the 7-Segment Display LEDs of each digit. SH only drives the first led digit to display the "[" symbol when the CPU is in calculation mode. Some TI59/58's and the TI58C have this line buffered by an extra transistor to enhance the output (remember that the D-lines are high only one quarter state-time on during calculation mode). Although my documentation was not clear on this I suspect the Segment-lines to be driven between Vss and –Vbat		??? Vss--Vbat (out)
Power bus	Vss	From Battery	0 Volt	
	-Vbat	From Battery	-3.7 Volt	
	Vdd	From Power module	-10 Volt	
	Vgg	From Power module	-15.7 Volt	

The following diagram shows a simplified representation of the way the calculator is wired (power, card reader and printer connections are not shown)

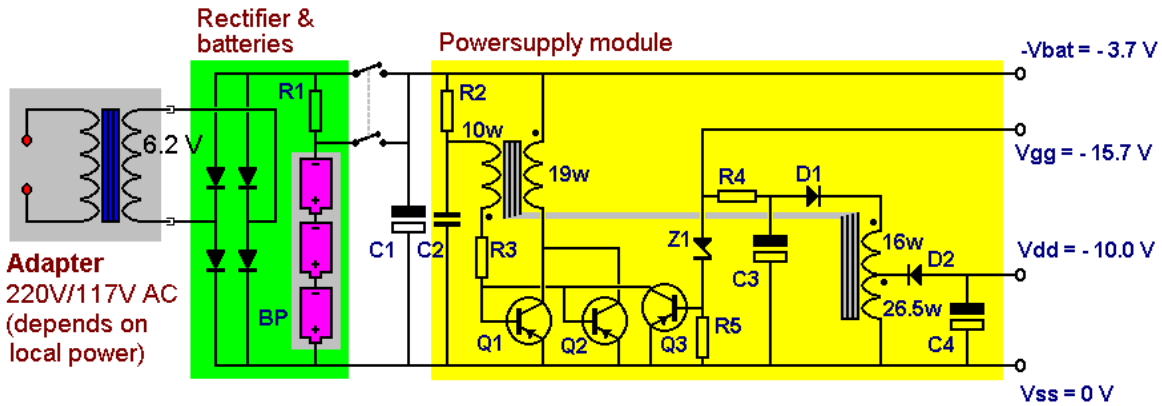
Abbreviated keyboard scanning and display drive circuit



φ1 & φ2 Clock timing diagram



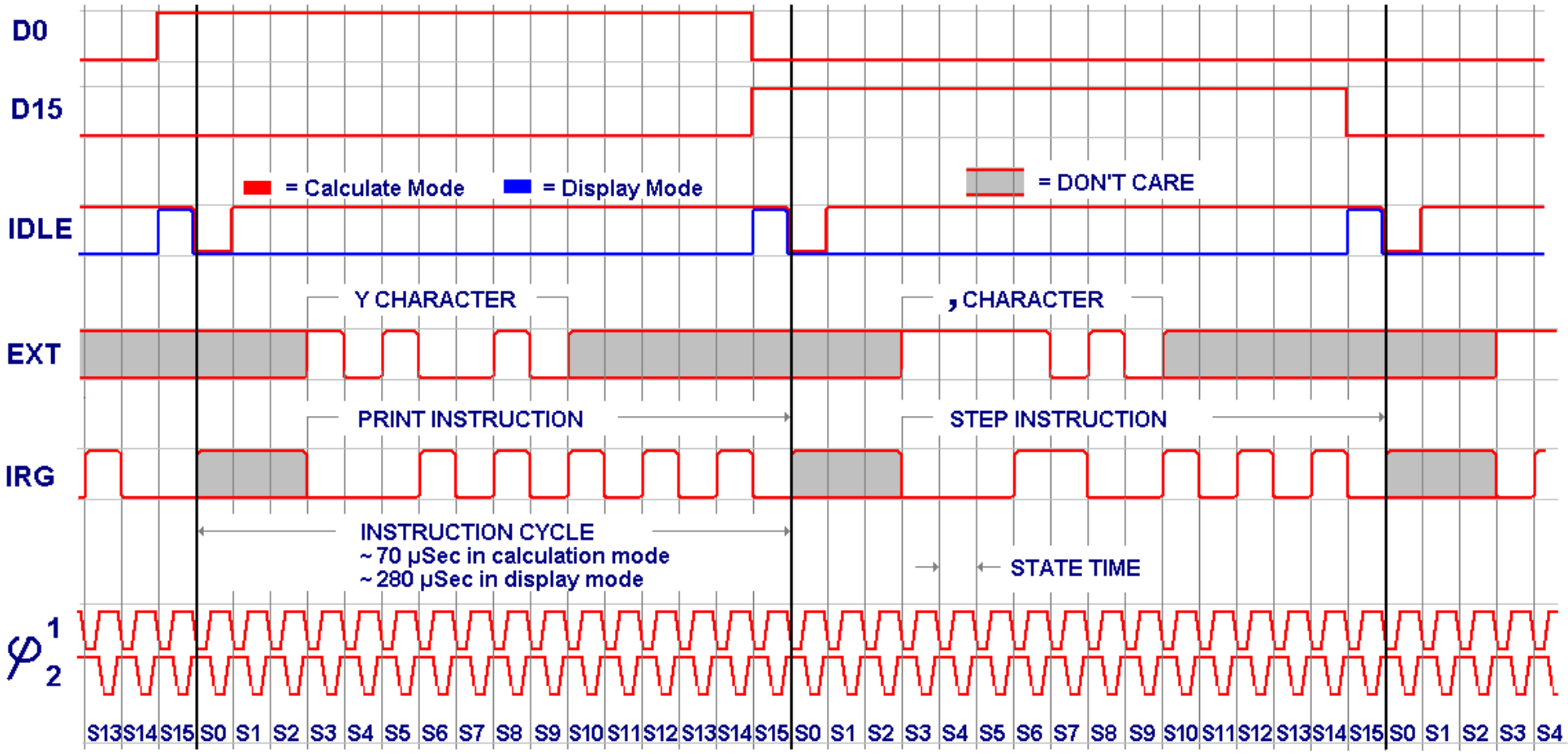
Below a small version of the TI59/58 Power supply diagram. (A larger version is available at my web-site)



R1 = 4.7 ohm	C1 = 47 uF	Q1, Q2 = QF2104
R2 = 270 ohm (150)	C2 = unkown (a few pF)	Q3 = QS9015B
R3 = 33 ohm	C3 = 22 uF	Z1 = 15.6 V
R4 = 820 ohm (1k2)	C4 = 33 uF	D1, D2 = 1N4150
R5 = 1k2		BP = BP1A

Sipke de Wal, April 2001

TI59/58 Timingdiagram



The Scanning ROMs

The table below shows the RAM-registers in the scanning ROMs. Beside RAM, the Scanning ROMs also contain 32 Constants in ROM and 2.5Kb ROM each.
“First ROM” is a part of the firmware (TMC 0571). “Second ROM” is the Library ROM: the First ROM -being equal to the Library ROM in connection method- contains part of the preprogrammed functions (Op functions) while the ROM in the scanning ROMs contain code for more primitive functions as a micro-code for the Arithmetic-chip.

TI59 CPU-registers

	Digit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
TMC0582 Registers	0	10 User Flags					0	0	0	RAM Address Second ROM Address			Byte	Prog SRC FLG	Last Key		Fix ptd	
	1	Mantissa													Exponent		Sign	Hierarchy Stack
	2																	
	3																	
	4																	
	5																	
	6																	
	7																	
TMC0583 Registers	8																	
	9	List of data flag	0	0	0	0	0	0	0	0	Current Page		New Page		Security Code	No of ROMs	No of prog banks	
	A	RAM or CONSTANT ROM PROGRAMCODES																
	B	T-REGISTER Mantissa													Exponent		Sign	
	C	PC 1	OP 1	PC 2	OP 2	PC 3	OP 3	PC 4	OP 4	PC 5	OP 5	PC 6	OP 6	PC 7	OP 7	PC 8	OP 8	Opcode & Par. Count for Hierarchy stack
	D	Page in run	0	0	0	0	0	0	RAM memory min. address			RAM memory max. address			No of pending ops	Parentheses count	Deg Rad Grd	
	E	Level 6 RAM Address Const &2nd ROM Address			Byte NR	Prog SRC FLG	Level 5 RAM Address Const &2nd ROM Address			Byte NR	Prog SRC FLG	Level 4 RAM Address Const &2nd ROM Address			Byte NR	Prog SRC FLG	Cond. Rtn Flag	Sup Routine Stack
	F	Level 3 RAM Address Const &2nd ROM Address			Byte NR	Prog SRC FLG	Level 2 RAM Address Const &2nd ROM Address			Byte NR	Prog SRC FLG	Level 1 RAM Address Const &2nd ROM Address			Byte NR	Prog SRC FLG	No of SBR levels	